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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/676,624	09/30/2003	William M. Siu	042390P6107D	7830
7590	03/03/2005			
Michael A. Bernadicou BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP Seventh Floor 12400 Wilshire Boulevard Los Angeles, CA 90025			EXAMINER PAREKH, NITIN	
			ART UNIT 2811	PAPER NUMBER

DATE MAILED: 03/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

**Office Action Summary**

Application No.

10/676,624

Applicant(s)

SIU ET AL.

Examiner

Nitin Parekh

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 30 September 2003.
- 2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 15-22 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 15-22 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 30 September 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)   | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)   | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152)             |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)<br>Paper No(s)/Mail Date <u>2</u> . | 6) <input type="checkbox"/> Other: _____  |

## DETAILED ACTION

### *Claim Objections*

1. Claims 20 and 22 are objected to because of the following informalities:

- A. The limitations as recited in claim 20, line 3, include "said second electrical connections have more routing channels extending therefrom than said first electrical connections".

However, as described in the specification and Figure 3 and 4, the first electrical connections (see 34/32a in Fig. 3) have more routing channels extending therefrom than those from the second electrical connections (see 32b in Fig. 3).

2. A. The limitations as recited in claim 22, line 2, include "wherein said first and second electrical connections are positioned on said surface in a progressive pitch layout".

However, as described in the specification and Figure 3 and 4, the second plurality of electrical connections (see 32b and 42b in Fig. 3 and 4 respectively) do not have positions having progressively increasing or decreasing spacing.

Appropriate correction is required.

***Claim Rejections - 35 USC § 102***

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 15-19 are rejected under 35 U.S.C. 102(b) as being anticipated by (Brandenburg et al.- see IDS reference US Pat. 5491364).

Regarding claims 15-19, Brandenburg et al. disclose a substrate such as a printed circuit board (PCB- see 14 in Fig. 1 and 4) comprising:

- the PCB substrate having a surface, the surface having a central region and an outer region (see the circumferential region including an array 28d and 28a respectively in Fig. 4)
- a first plurality of electrical connections on the outer region spaced apart by a first distance (see spacing between 28a in Fig. 4), and
- a second plurality of electrical connections on the central region spaced apart by a second distance (see spacing between 28d in Fig. 4), wherein said second distance is smaller than said first distance (Col. 6, lines 5-9), and
- the electrical connections including input/output (I/O) connections having the array of terminals/pads, electrically conductive bumps/solder bumps,

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pads/conductive lands, solder pins/connector pins, etc. (Col. 5, lines 2-63; Col. 4-7)

(Fig. 4; Fig. 1-5; Col. 1-7).

Regarding claim 20, Brandenburg et al. teach the entire structure as applied to claim 15 above, wherein Brandenburg et al. teach the plurality of electrical connections having routing conductors/channels extending therefrom (see 34 in Fig. 5), the routing pattern being such that the first electrical connections have more routing conductors/channels than those from the second electrical connections (see 34 extending from 28a versus those from 28d in Fig. 5).

### ***Claim Rejections - 35 USC § 103***

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

6. Claims 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over (Brandenburg et al. - see IDS reference US Pat. 5491364) in view of Johnson et al. (see IDS reference US Pat. 4495377).

Regarding claim 21, Brandenburg et al. teach substantially the entire structure as applied to claim 15 above, wherein Brandenburg et al. teach the second plurality of electrical connections not having any routing channel between them (see the pattern of 34 in Fig. 5), but Brandenburg et al. fail to teach the first plurality of electrical connections having at least four routing channels passing between them.

Johnson et al. teach a substrate having a variety of array of a plurality of electrical connections including pads/terminals and respective wiring/routing conductors (see 12 and 13 respectively in Fig. 1) including the configuration (see Fig. 1) where the plurality of electrical connections in an outer region have more than four conductor patterns/routing channels passing between to provide the increased number of conductors in straight line configuration, having thinner conductors and optimized pad/conductor spacing layout (Col. 2, line 15-35).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the first plurality of electrical connections having at least four routing channels passing between them as taught by Johnson et al. so that the conductor density can be increased, the resistance can be reduced and the desired I/O and power connections can be achieved in Brandenburg et al's PCB.

Regarding claim 22, Brandenburg et al. teach substantially the entire structure as applied to claim 15 above, except the first and second electrical connections being positioned in a progressive pitch layout.

Johnson et al. teach array of a plurality of electrical connections having concentric array/layout where pitch/spacing of the electrical connections/pads is progressively reduced from the first electrical connections/pads in an outer region to the second electrical connections/pads in the central region (see spacing between 12 in Fig. 1).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the first and second electrical connections being positioned in a progressive pitch as taught by Johnson et al. so that the conductor density and routing can be improved and the shorting can be reduced in Brandenburg et al's PCB.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 571-272-1663. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9318.

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Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

NP

02-28-05



NITIN PAREKH

PRIMARY EXAMINER

TECHNOLOGY CENTER 2800